# Single-Phase to Three-Phase Converters With Two Parallel Single-Phase Rectifiers and Reduced Switch Count

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Abstract- This paper presents two single-phase to threephase conversion systems for a three-phase load application. The load is connected to a single-phase grid through an AC-DC-AC single-phase to three-phase converter. The single-phase rectifier is composed of two parallel singlephase half-bridge rectifiers. The first proposed topology is composed of a full-bridge three-phase inverter, i.e., threeleg inverter, while the other topology is composed of a twoleg inverter. Suitable modelling, including the circulation current, and control strategy are presented. A pulse widthmodulation (PWM) technique using a single or double carriers PWM implementation is presented. Proposed topologies permit to improve the harmonic distortion. In addition, it can reduce the converter power losses. Finally, simulation and experimental results are presented for validation purposes.

## I. INTRODUCTION

Brazil is a country with continental dimensions and in some regions (rural areas or remote locations) the power distribution system is typically a single-phase type. The cost to change from a single-phase to a three-phase power system is often high due to the high cost associated with a three-phase extension [1]. In rural or remote areas, the use of three-phase induction machines is preferred instead of single-phase induction machines due to its advantages such as low cost, lower volume, redundancy, etc. [1–3]. However, even if a three-phase voltage source is available, a power converter is needed to allow speed or torque control of the induction motor drive. But, if only a single-phase utility is available, a single-phase to three-phase (1ph-to-3ph) converter is indispensable to feed a three-phase motor. Furthermore, nowadays some rural loads, e.g., electronic power converters, computers, communications equipment, etc., demand high power quality with sinusoidal balanced three-phase voltages [4], [5].



Fig. 1. Conventional 1ph-to-3ph converter systems. (a) Five legs (5L) converter. (b) Four legs (4L) converter. (c) Three legs (3L) converter.

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The 1ph-to-3ph power converter based on a full-bridge diode rectifier is a standard solution [1]. However, this solution provides high harmonic distortion and a low power factor. To solve this problem, a controlled rectifier in place of the diode rectifier is required. Such an alternative solution can provide low harmonic distortion and a high power factor to the grid. The 1ph-to-3ph converter based on a controlled rectifier is composed of five legs (ten controlled power devices), as shown in Fig. 1(a). It is denominated conventional 5L converter.

In order to reduce the cost and power losses in the power converter, different configurations of 1ph-to-3ph converter with a reduced number of power devices have been proposed in the literature [1], [6–14].

Within that range of possibility, we can highlight the configurations with four legs (composed of a full-bridge rectifier and a three-leg inverter with a shared-leg), denominated here conventional 4L converter [see Fig. 1(b)], and the configuration using three legs (composed of a half-bridge rectifier and two-leg inverter), denominated here conventional 3L converter [see Fig. 1(c)]. The 4L converter is proposed in [9]. The 4L converter uses less switches than the full-bridge 5L converter, but its DC-link voltage rating is equal to the 3L converter. For 4L converter, using constant frequency output voltage and suitable control strategy, the DC-link voltage rating is the same as the conventional 5L counterpart [9]. The conventional 3L power converter uses only six power switches instead of ten of the conventional full-bridge 5L power converter. However, increases the harmonic distortion of input current and twice of the DC-link voltage is required [8], [10], [12].

With the reduction of the cost of the power switches new topologies using a larger amount of power switches have been proposed [15–21]. Parallel converters are a promising solution for 1ph-to-3ph conversion systems, due to the reduction of irregular distribution of power losses among the switches of both rectifier and inverter, with the reduction of the current processed by rectifier switches [22]. Additionally, the interleaved technique can still be employed to improve the harmonic distortion, reliability, and efficiency of parallel converters [16–19].

In [19] a 1ph-to-3ph converter system, with a parallel fullbridge rectifier circuit, is considered to reduce the current processed by rectifier switches. This configuration improves the harmonic distortion and efficiency at the rectifier side, however it is composed of seven legs (a total of fourteen power switches) denominated 7L configuration, as shown in Fig. 2(a). An intermediate alternative between the configuration presented in [19] and the configuration 4L is proposed in [20]. This configuration is composed of two parallel full-bridge rectifiers with a shared-leg between the inverter and rectifier circuits, it uses a total of ten power switches, known as 5La converter, as shown in Fig. 2(b).

In general the AC-DC-AC converter are designed by connection between known rectifier and inverter circuits, with exception of AC-DC-AC converters using a shared-leg. This paper addresses two topologies of power converter to 1ph-to-3th conversion system. The rectifier side uses two parallel legs (each leg represents a half-bridge rectifier), as shown in Fig. 3. The first topology presents five legs, i.e., P5L converter [see



Fig. 2. Parallel 1ph-to-3ph converter. (a) With parallel full-bridge rectifiers (seven legs denominated as 7L). (b) Parallel rectifier with a shared-leg (Five leg denominated as 5La).

Fig. 3(a)] and the second one uses four legs, i.e., P4L converter [see Fig. 3(b)]. The topology P5L was proposed in [23]. In fact, the proposed topologies are obtained by the addition of two parallel half-bridge rectifier with two known inverter circuits. However, these topologies can improve the overall performance of AC-DC-AC converter, such as the harmonic distortion and efficiency, when compared to topologies with a close number of switches (conventional 5L and 3L converter). These topologies improve the division of power flow between the inverter and rectifier switches, which can reduce the power losses at the rectifier circuits. They are also more economically attractive, with lower cost, because they use a smaller amount of power devices in comparison with the 7L converter. Suitable modelling, control strategy and circulation current control are presented for validation purposes.

Among topologies addressed in this paper, the P5L topology presents the best performance, because it can reduce: i) power losses in switches, due to a reduction of the current in rectifier circuit and ii) the harmonic distortion on the utility grid, when the interleaved technique is applied. The P4L topology reduces the harmonic distortion compared by 3L converter and provides the same harmonic distortion of the conventional 5L counterpart in the single-phase grid, when the interleaved technique is also adopted. The output three-phase AC voltages of the proposed systems can be variable, to supply a motor with variable voltages for achieving its speed and torque control, or with constant amplitude and frequency, to supply

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Fig. 3. Proposed 1ph-to-3ph converter using a half-bridge rectifier circuit. (a) Parallel five legs (P5L) converter. (b) Parallel four legs (P4L) converter.

constant three-phase load type.

The paper is organized as follows. Section II, the system model is presented. The control system and Pulse-Width Modulation (PWM) strategy are discussed in Sections III and IV, respectively. In Sections V, VI and VII the main figures of merit used in the comparison of the topologies discussed in this paper are analysed, i.e.,: 1) DC-link voltage rating, 2) rectifier harmonic distortion, and 3) converter power losses, respectively. The simulation and experimental results are presented in Sections VIII and IX, respectively. Finally, in Section X, the brings up the conclusions are made.

# II. SYSTEM MODEL

The P5L configuration presented in Fig. 3(a) is composed of two single-phase half-bridge rectifiers (rectifiers A and B), a DC-link, a three-phase inverter and a three-phase motor or a three-phase load. On the other hand, the P4L configuration [Fig. 3(b)] is composed of a two-leg inverter instead three-leg inverter of the P5L converter.

# A. Rectifier Model

From Fig. 3 the following model is derived:

$$e_g = r_{g1}i_{g1} + l_{g1}\frac{di_{g1}}{dt} + v_{g10}$$
(1)

$$e_g = r_{g1}i_{g2} + l_{g1}\frac{di_{g2}}{dt} + v_{g20}$$
(2)

$$i_g = i_{g1} + i_{g2}$$
 (3)

where  $r_{g1}$  represents the resistance of the inductor filter  $L_{g1}$ ,  $l_{g1}$  represents the inductance of the inductor filter  $L_{g1}$ ,  $v_{g10}$ 

and  $v_{g20}$  are the pole voltages of the rectifiers A and B, respectively,  $i_g$  is the grid current and  $i_{g1}$  and  $i_{g2}$  are the input currents of the rectifiers A and B, respectively.

The previous model can also be expressed by using the circulating current  $i_o$  introduced by

$$i_{g1} = \frac{i_g}{2} + i_o$$
 (4)

$$i_{g2} = \frac{i_g}{2} - i_o$$
 (5)

From (1) to (5), the complete system model is given by

$$e_g = \left(\frac{r_{g1}}{2}\right)i_g + \left(\frac{l_{g1}}{2}\right)\frac{di_g}{dt} + v_g \tag{6}$$

$$v_o = r_{g1}i_o + l_{g1}\frac{di_o}{dt} \tag{7}$$

with

6

$$i_o = \frac{i_{g1} - i_{g2}}{2}$$
 (8)

$$v_g = \frac{v_{g10} + v_{g20}}{2} \tag{9}$$

$$v_o = \frac{-v_{g10} + v_{g20}}{2} \tag{10}$$

From (6) to (10) it is clear that the grid and circulating currents depend on the voltages  $v_g$  and  $v_o$ , respectively. Then, the rectifier pole voltages can be calculated from desired voltages ( $v_g$  and  $v_o$ ) to control these currents. Considering circulating current null and the equivalent inductor  $L_g = L_{g1}/2$  equal to that of the conventional converter, the front-end model of the configurations presented in Fig. 3 is identical to that of the conventional 5L converter.

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## B. Inverter Model

The inverter model for the P5L configuration is given by

$$v_{s1} = v_{s10} - v_{n0} \tag{11}$$

$$v_{s2} = v_{s20} - v_{n0} \tag{12}$$

$$v_{s3} = v_{s30} - v_{n0} \tag{13}$$

where  $v_{s10}$ ,  $v_{s20}$  and  $v_{s30}$  are the pole voltages of the inverter,  $v_{s1}$ ,  $v_{s2}$  and  $v_{s3}$  are the voltages of the three-phase load, and  $v_{n0}$  is the voltage between the point n and the DC-link midpoint 0.

While the model of inverter of the P4L configuration is given by

$$v_{s13} = v_{s10}$$
 (14)

$$v_{s23} = v_{s20}$$
 (15)

where  $v_{s13}$  and  $v_{s23}$  are line voltages of the three-phase load.

# **III. CONTROL STRATEGY**

The control system of the proposed converters has the same objectives of the conventional one, i.e., DC-link voltage and power factor control from rectifier circuit and load voltage control from inverter circuit. Additionally, the proposed control system needs to regulate the circulating current between the parallel half-bridge rectifiers. Fig. 4 shows the control block diagram of the P5L and P4L converters proposed in this paper. The capacitor DC-link voltage  $E_d$  ( $E_{d1} + E_{d2}$ ) is adjusted to its reference value  $E_d^*$  utilizing a PI (Proportional Integral) type controller. This controller provides the amplitude of the reference grid current  $I_q^*$ . To control power factor and harmonics at the grid side, the instantaneous reference grid current  $i_{qx}^*$  must be synchronized with the grid voltage  $e_g$ based on PLL (Phase Locked Loop) scheme [24]. Control of the grid current is implemented using a synchronous controller (a resonant controller type) described in [25]. The block  $R_q$ represents this controller. It defines the reference grid voltage

The circulating current  $(i_o)$  is obtained by block  $G_{pio}$  from the measured rectifiers currents  $i_{g1}$  and  $i_{g2}$ . This block is based on equation (8). The circulating current is compared to its reference  $(i_o^* = 0)$ . The error is the input of a synchronous controller  $(R_o)$ , and gives in its output the voltage  $v_o^*$ .

Due to different dead-time switches, non-sinusoidal grid voltage or different capacitance, the voltage balance between the split capacitors obtained naturally may not be satisfactory. Some works have proposed solutions to voltage balance between the split capacitors of the half-bridge rectifier [26–29]. One way to minimize the voltage imbalance between split capacitors is to add a current balance value  $i_{bal}^*$  in the reference grid current. The difference in voltage between the split capacitors ( $E_{d1} - E_{d2}$ ) is input of the conventional PI controlled. This controller provides the reference current balance value  $(i_{bal}^*)$ . The reference grid current is achieved by adding  $i_{gx}^*$ with  $i_{bal}^*$  ( $i_g^* = i_{gx}^* + i_{bal}^*$ ), as discussed in [27]. The voltage balance between the split capacitors is carried out, but it is necessary to apply a small distortion in the reference grid current.



Fig. 4. Control block diagram used for configurations P5L and P4L.

When a three-phase motor is used, control can be performed by field oriented control (FOC) technique as shown in [30] or volt/hertz control.

# IV. PWM STRATEGY

The PWM methods can be based on classic sinusoidal modulation, scalar as well as on vector modulation approach [31], [32]. In sinusoidal modulation, the gating signals are obtained by comparing reference pole voltages with a triangular carrier signal. In this paper, the PWM strategy for the rectifiers A and B will be based on sinusoidal modulation. The gating signals are obtained by comparing reference pole voltages with one or two high-frequency triangular carrier signals [31], i.e., a single or double carriers PWM implementation. In the case of double-carrier approach (interleaved technique), the phase shift of the two triangular carrier signals is 180°. The reference pole voltages of the rectifiers are obtained as follows.

Considering that  $v_g^*$  and  $v_o^*$  are the reference voltages determined by the current controllers (see Section III), from equations (9) and (10) we found

$$v_g^* = \frac{v_{g10}^* + v_{g20}^*}{2} \tag{16}$$

$$v_o^* = \frac{-v_{g10}^* + v_{g20}^*}{2} \tag{17}$$

Writing (16) and (17) in matrix form

$$\begin{bmatrix} v_g^* \\ v_o^* \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} v_{g10}^* \\ v_{g20}^* \end{bmatrix}$$
(18)

The gating signals are directly calculated from the reference pole voltages  $(v_{q10}^* \text{ and } v_{q20}^*)$ , solving (18), we obtain

$$\begin{aligned}
 v_{g10}^* &= v_g^* - v_o^* & (19) \\
 v_{g20}^* &= v_g^* + v_o^* & (20)
 \end{aligned}$$

Suitable modulation is obtained when  $-E_d^*/2 \leq v_{g10}^* \leq E_d^*/2$  and  $-E_d^*/2 \leq v_{g20}^* \leq E_d^*/2$ . Where  $E_d^*$  is the reference DC-link voltage with  $E_d^* = E_{d1}^* + E_{d2}^*$ .

The three-phase inverter (P5L configuration) can be commanded by using an adequate PWM strategy for three-phase voltage source inverter (VSI) [32]. While for the two-leg inverter (P4L converter) the PWM can be obtained with a similar technique presented in [29], [33].

# V. DC-LINK CAPACITOR

## A. DC-Link Capacitor Voltage

Considering that all the voltages are purely sinusoidal, the voltage limit conditions of each configuration is shown in the Table I. Where  $V_g$  represents the amplitude of rectifier voltage, whereas  $V_s$  denotes the amplitude of the load phase voltage.

TABLE I DC-LINK VOLTAGE LIMITS.

Configurations	Input Limit	Output Limit
5L	$E_d \ge V_g$	$E_d \ge \sqrt{3}V_s$
3L	$E_d \ge 2V_g$	$E_d \ge 2\sqrt{3}V_s$
P5L	$E_d \ge 2V_g$	$E_d \ge \sqrt{3}V_s$
P4L	$E_d \ge 2V_g$	$E_d \ge 2\sqrt{3}V_s$

If the input voltage is equal to output voltage (i.e.,  $V_g = V_s$ ) the conventional 5L converter has the best DC-link voltage rating. The proposed P5L converter has the DC-link voltage 15% bigger than the conventional 5L one. While conventional 3L and proposed P4L converters require twice the DC-link voltage of the conventional 5L one.

On the other hand, when the output voltage is double the input voltage (i.e.,  $V_s = 2V_g$ ), the proposed P5L converter can operate with the same DC-link voltage of the conventional 5L converter.

# B. DC-Link Capacitor Current

From Fig. 3(a), the DC-link capacitor current for the P5L converter can be given by

$$i_{c1} = \sum_{k=1}^{2} \frac{\tau_{gk}}{T_s} i_{gk} - \sum_{j=1}^{3} \frac{\tau_{sj}}{T_s} i_{sj}$$
(21)

$$i_{c2} = -\sum_{k=1}^{\infty} \left(1 - \frac{\tau_{gk}}{T_s}\right) i_{gk} + \sum_{j=1}^{\infty} \left(1 - \frac{\tau_{sj}}{T_s}\right) i_{sj} (22)$$

where  $\tau_{gk}$  and  $\tau_{sj}$  are the time intervals in which switches  $q_{gk}$ and  $q_{sj}$  are closed (with k = 1, 2 and j = 1, 2, 3), respectively, and  $T_s$  is the sampling time. Assuming that the reference pole voltages are constant over  $T_s$ , the time intervals  $\tau_{gk}$  and  $\tau_{sj}$ can be written as a function of the reference pole voltages. For instance,  $\tau_{gk}$  is given by

$$\tau_{gk} = \left(\frac{v_{gk0}^*}{E_d^*} + \frac{1}{2}\right) T_s$$
(23)

Thus, from (23), (21) and (22) the DC-link capacitor current

is given by

$$i_{c1} = \frac{i_g}{2} + \sum_{k=1}^{2} \frac{v_{gk0}^*}{E_d^*} i_{gk} - \sum_{j=1}^{3} \frac{v_{sj0}^*}{E_d^*} i_{sj}$$
(24)

$$i_{c2} = -\frac{i_g}{2} + \sum_{k=1}^{2} \frac{v_{gk0}^*}{E_d^*} i_{gk} - \sum_{j=1}^{3} \frac{v_{sj0}^*}{E_d^*} i_{sj}$$
(25)

If the reference pole voltages are defined by equations (19) and (20) and the rectifier currents by equations (4) and (5), then the capacitor currents  $i_{c1}$  and  $i_{c2}$  can be written as follows:

$$i_{c1} = \frac{i_g}{2} + \frac{v_g^*}{E_d^*} i_g - \frac{2v_o^*}{E_d^*} i_o - \sum_{j=1}^3 \frac{v_{sj}^*}{E_d^*} i_{sj}$$
(26)

$$i_{c2} = -\frac{i_g}{2} + \frac{v_g^*}{E_d^*}i_g - \frac{2v_o^*}{E_d^*}i_o - \sum_{j=1}^3 \frac{v_{sj}^*}{E_d^*}i_{sj}$$
(27)

The first component of the capacitor currents, for P5L converter, is due to the grid connection at the midpoint of the DClink, the second component is due to the single-phase voltage source, with twice of the grid frequency. The third component is a consequence of the circulating current. Although there is no low frequency circulating current (eliminated by controller) it may exist with high frequency circulating current due to the interleaving technique. The last term is due to the three-phase inverter.

A similar analysis may be obtained with P4L converter, but in this case, there is a load current component  $(i_{s3})$  due to the load connection at the midpoint DC-link, as shown in (28) and (29).

$$i_{c1} = \frac{i_g}{2} + \frac{i_{s3}}{2} + \frac{v_g^*}{E_d^*} i_g - \frac{2v_o^*}{E_d^*} i_o - \sum_{j=1}^2 \frac{v_{sj0}^*}{E_d^*} i_{sj} \quad (28)$$

$$i_{c2} = -\frac{i_g}{2} - \frac{i_{s3}}{2} + \frac{v_g^*}{E_d^*}i_g - \frac{2v_o^*}{E_d^*}i_o - \sum_{j=1}^2 \frac{v_{sj0}^*}{E_d^*}i_{sj}$$
(29)

Fig. 5 shows the harmonic spectrum of capacitor currents. These results have been obtained with the parameters shown in Table III, with load line voltage equal to 220V/60Hz, load power equal to 1.5kVA and the power factor equal to 0.8 lagging. The P5L, P4L and 3L converters have a low frequency component at 60Hz (grid/load), because the midpoint of DC-link voltage is shared with the grid and/or three-phase load. If the electrical machine is operating with variable speed, P4L and 3L converters will have a harmonic component in machine frequency (not shown in figure because both grid and three-phase load frequencies are equal to 60Hz).

Another common feature among the studied configurations is a component in frequency of 120Hz due to a singlephase power supply. Moreover, the proposed configurations have a reduction at high frequency components in capacitor currents, especially when double-carrier PWM is applied. For instance, the RMS capacitor current of the P5L converter (with interleaved technique) decreases by 33% compared to conventional 5L converter.

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Fig. 5. Simulation results - Spectrum of the DC-link capacitor current. (a) 5L converter. (b) 3L converter. (c) P5L converter with single-carrier PWM (P5L1). (d) P5L converter with double-carrier PWM (P5L2). (e) P4L converter with single-carrier PWM (P4L1). (f) P4L converter with double-carrier PWM (P4L2).



Fig. 6. Simulation results - WTHD of the rectifier voltage for different switching frequencies. (a) 4kHz. (b) 6kHz. (c) 8kHz. (d) 10kHz.

#### VI. HARMONIC DISTORTION

In this paper the weighted total harmonic distortion factor (WTHD) has been used to evaluate the distortion of converter voltage, because it is superior to the THD (total harmonic distortion factor) to measure the quality of a non-sinusoidal waveform [34]. The WTHD is defined by

$$WTHD = \frac{\sqrt{\sum_{h=2}^{N_h} \left(\frac{V_h}{h}\right)^2}}{V_1}$$
(30)

where  $V_1$  is the amplitude of the fundamental voltage component,  $V_h$  is the amplitude of  $h^{th}$  component voltage harmonic and  $N_h$  is the number of harmonics taken into consideration.

The WTHD value has been obtained from digital simulation. The simulation was developed for the mathematical model and the PWM strategy described in Sections II and IV, respectively. The simulation tool used was Matlab<sup>(R)</sup>. The simulation model was obtained from the parameter presented in Table II with  $v_o^*$  equal to zero.

TABLE II Parameter of WTHD analysis.

Voltage Rating	127V(RMS)	Power Rating	1.5kVA
Grid Voltage	1.0 pu	Load Voltage	1.0 pu
Power Factor	0.8 (lagging)	Load Current	1.0 pu
$r_g$	0.01 pu	$x_g$	0.1 pu

Fig. 6 shows the WTHD of the rectifier voltages for the proposed P5L [with single-carrier (P5L1) and double-carrier PWM (P5L2)], proposed P4L [with single-carrier (P4L1) and double-carrier PWM (P4L2)], conventional 5L and conventional 3L configurations for different switching frequencies  $(f_{sw})$ . In this analysis the equivalent inductor  $L_g = L_{g1}/2$  is equal to that of conventional converters,  $V_g = V_s$  and the DC-link voltage is obtained from the Table I.

From Fig. 6 is possible to make the following conclusions:

- The WTHD of the proposed P4L converter with singlecarrier PWM (P4L1) is always equal to the WTHD of the conventional 3L one.
- The highest values of WTHD are obtained with P4L1 and 3L configurations.
- The best values of WTHD are obtained with the proposed P5L converter with double-carrier PWM (P5L2).
- The WTHD of the proposed P4L converter with doublecarrier PWM (P4L2) is equal to the WTHD of the conventional 5L one.
- The WTHD value of the P5L2 is always smaller than the WTHD of the conventional 5L converter.
- Additionally, when  $f_{sw} > 4$ kHz the WTHD of the proposed P5L2 converter is smaller than the WTHD conventional 5L one with  $f_{sw} = 10$ kHz.

In fact, when we use the interleaved technique (doublecarrier PWM), the P5L and P4L configurations provide a re-

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Fig. 7. Highlighting the PWM strategy implementation. (a) Conventional converters. (b) P5L converter. (c) P4L Converter.

duction in harmonic distortion of the voltage  $v_g$ , consequently in the grid current [see equation (6)]. As shown in [31], this technique does not affect the amplitude of harmonic components, but can change the phase of the harmonic component between parallel converters at the same frequency. Towards a better understanding of the WTHD analyses, Fig. 7 shows the detail of modulation of all topologies addressed in this paper. In this figure, the triangular carriers PWM ( $v_{t1}$  and  $v_{t2}$ ), the pole voltages ( $v_{g10}^*$ ,  $v_{g20}^*$ ,  $v_{g10}$  and  $v_{g20}$ ), and rectifier voltage ( $v_g$ ) during a switching period  $T_{sw}$  is highlighted.

All the signals are normalized by the DC-link voltage of the conventional 5L converter. For instance, for P5L converter the amplitude of the triangular signal is between -0.58 and 0.58, because the DC-link voltage is 15% greater that the 5L converter, while for 3L or P4L converters, the amplitude is between -1.0 to 1.0, because the DC-link voltage is the double. For both proposed configurations, with single-carrier PWM, the pulse of waveform voltage  $v_g$  is not well distributed in half period of switching which increases the WTHD value. With a single-carrier PWM, the voltages of the parallel legs ( $v_{g10}$  and  $v_{g20}$ ) are the same, so there is no circulating voltage  $v_o$  and there is no cancellation of harmonic components. Furthermore, for P4L converter, the waveform of  $v_g$  is identical to the 3L converter, thus justifying the same WTHD value.

A better distribution of generated pulses by voltage  $v_g$  is

achieved when double-carrier PWM is applied. In the P5L configuration the pulse of voltage  $v_g$  is centralized in half period of switching and the amplitude of  $v_g$  is smaller than that of the conventional 5L converter. This feature ensures a reduction in WTHD value, as presented in Fig. 6. While for P4L converter, the waveform of  $v_g$  is equal to the conventional 5L converter, this explains the same WTHD value. With double-carrier PWM, since the waveforms of the voltages  $v_{g10}$  and  $v_{g20}$  are different, the phase angle of harmonic voltages changes, so there is cancellation of harmonic components of voltage  $v_g$ , as well, there will be the voltage  $v_o$  which produces the circulating current [see Figs. 7(b) and 7(c)].

#### VII. CONVERTER LOSSES

Several studies have been performed in order to determine the power losses in the power switches (IGBTs and MOS-FETs) [35–39]. Two solutions are generally applied: i) the experimental measurement of power loss, with the aim of constructing mathematical functions from a regression model and ii) determining losses using linear IGBT and diode models. In this paper, the losses estimation is obtained through of the regression model, which has been achieved by experimental tests. The tests were performed for different values of currents and temperatures. All data of losses have been employed to obtain the regression model, as presented in [38], [39]. Such a regression model provides polynomial equations for the losses.

The instantaneous losses function of an IGBT dual module CM50DY-24H manufactured by POWEREX driven by driver SKHI-10 manufactured by SEMIKRON was determined. Then, digital simulation provided by PSIM<sup>®</sup> simulation software was used to calculate the power losses in converters. The polynomial equations were implemented using a DLL written in C (programming language).

Fig. 8 shows the semiconductor power losses for conventional and proposed topologies obtained using switching frequency equal to 10kHz. The DC-link voltages are defined by the Table I, with  $V_g = V_s$ . The load line voltage is equal to 220V/60Hz and the load power is equal to 4.5kVA with the power factor equal to 0.8 lagging. Other parameters are addressed in Table III.

 TABLE III

 PARAMETER FOR POWER LOSSES ESTIMATION.

Parameter	Value		
DC-Link Voltage (5L)	346V		
DC-Link Voltage (P5L)	399V		
DC-Link Voltage (3L)	691V		
DC-Link Voltage (P4L)	691V		
DC-Link Capacitance	1100uF		
Grid Voltage	127V(RMS)		
$r_g$	0.1Ω		
$l_g$	3mH		

Figs. 8(a), 8(b) and 8(c) present the conduction, switching and total power losses estimation, respectively, as a percentage of load power. In these figures, we can see that the proposed P5L converter provides a reduction in total power losses compared with the other configurations. However, the proposed P4L configuration has the worst performance in this criterion.

As shown in [38], the regression model of conduction losses is a function of the leg current, while the model of the switching losses is function of DC-link voltage and leg current of the converter. Table IV illustrated the current rating in the rectifier leg normalized by the current of the conventional 5L configuration. Notice that, the current in proposed topologies is almost half of conventional ones. Regardless of 3L and 4L converters having a smaller number of power switches, they need a DC-link voltage value that is twice the conventional 5L one. Therefore, the switching losses are higher than that of conventional 5L converter.

Fig. 8(d) shows the average power losses in each leg of converters (rectifier and inverter) normalized by the total power losses. In fact, the reduction of the current processed by rectifier switches provides a mitigation in an irregular distribution of power losses among the switches of the rectifier and inverter. This could allow the application of the same switches in the rectifier and inverter circuits. Furthermore, due to the non-linear model of the power switches, even reducing the currents in almost 50%, for P4L converter, the total loss in the rectifier circuit is greater than the 3L converter [see Fig. 8(d)], thus justifying its worst performance among the studied configurations.



Fig. 8. Simulation results of semiconductor power loss estimation. (a) Conduction losses. (b) Switching losses. (c) Total losses. (d) Average losses in each leg of the converter.

TABLE IV CURRENT RATINGS IN THE RECTIFIER LEG.

5L	3L	P5L	P4L
100.0%	106.1%	49.9%	51.85%

## VIII. SIMULATION RESULTS

In order to demonstrate the feasibility of the proposed topologies, digital simulations have been performed. The results are obtained to the following conditions: DC-link voltage equal to 400V (P5L converter) and 691V (P4L converter), grid voltage equal to 127V, an induction machine of 2kW (220V/60Hz), and the switching frequency equal to 10kHz. These results are obtained with double-carrier PWM and Volt/Hertz control with machine frequency equal to 30Hz.

Figs. 9 and 10 show the simulation results for P5L and P4L configurations, respectively. Notice that the grid current is sinusoidal with power factor close to one [see Figs. 9(a) and 10(a)], the DC-link voltage is controlled [as shown in Figs. 9(a) and 10(a)] and the circulating current is null [see Figs. 9(c) and 10(c)]. Fig. 9(a) shows the DC-link voltage for P5L converter. Notice that, a low-component frequency of grid current and a second harmonic component appear in the DC-link voltage. On the other hand, for P4L configuration [see Fig. 10(a)] in addition to the aforementioned components, there is a low-frequency component of load current. A higher value of capacitance to the DC-link can mitigate this swinging. Furthermore, these configurations provide a current reduction in the single-phase rectifiers (half of the current of the standard topology) [see Figs. 9(b) and 10(b)], which can provide a reduction of the power losses.

## IX. EXPERIMENTAL RESULTS

The proposed systems have been implemented in the laboratory. Steady-state operation mode has been considered in the experimental tests. The experimental set-up is based on two

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Fig. 9. Simulation results of the P5L2 converter. (a) Top: voltage and current of the grid, bottom: DC-link voltage. (b) Top: input current of the Rectifier A, bottom: input current of the Rectifier B. (c) Top: circulating current, bottom: load currents.



Fig. 10. Simulation results of the P4L2 converter. (a) Top: voltage and current of the grid, bottom: DC-link voltage. (b) Top: input current of the Rectifier A, bottom: input current of the Rectifier B. (c) Top: circulating current, bottom: load currents.

sets of SEMIKRON manufacturer (each set consists of a power converter of three branches based on IGBT SKM50GB123Dswitches and a capacitor bank with access to the central point), and a Digital Signal Processor (DSP) TMS320F28335 with a microcomputer equipped with appropriate plug-in boards and sensors, as addressed in Fig. 11. The results were obtained by an oscilloscope *Agilent* DSO-X 3014A 100MHZ. The following parameters were used: inductor filters equal to 6mH, DC-link capacitance equal to 4400 $\mu$ F, DC-link voltage 190V (for P5L converter) and 240V (for P4L converter), grid voltage 40V, an induction machine of 1.5cv (220V/60Hz), and switching frequency equal to 10kHz. A Volt/Hertz machine control with machine frequency equal to 20Hz were used to obtain these results.

Notice that, all control requirements have been established, i.e., the control guarantees sinusoidal grid current with power factor close to one [see Figs. 12(a) and 13(a)] and DC-link voltage under control [see Figs. 12(c) and 13(c)]. The control guarantees the circulating current close to zero [see Figs. 12(b) and 13(b)]. Additionally, the proposed configurations provide



Fig. 11. Photo of experimental Set-up, DSP and a three-phase induction machine.

reduction currents of the rectifier circuit. In fact, the currents of the rectifiers A and B ( $i_{g1}$  and  $i_{g2}$ ) are half of the current of the conventional one. Fig. 12(d) shows the DC-link voltages of split capacitors for P5L converter. In this case, a low-frequency component of grid current and a second harmonic (due to single-phase source) appear in both DC-link voltages ( $E_{d1}$ )



Fig. 12. Experimental results of the P5L2 converter. (a) Voltage and current of the grid. (b) Input currents of rectifiers A and B and circulating current. (c) DC-link voltage and load currents. (d) DC-link voltages.

and  $E_{d2}$ ), while the total DC-link voltage  $E_d$  remain almost constant. Fig. 13(d) shows that a low-frequency component of load current appears in both DC-link voltages ( $E_{d1}$  and  $E_{d2}$ ) in addition to the low-frequency component of grid current and the 120Hz component. The performance of the proposed systems is adequate.

Fig. 14 shows the capacitor current  $(i_{c1})$  in the frequency domain for the same set of experimental results presented in Figs. 12 and 13. These results are obtained with single and double-carrier PWM. Notice that, both configurations have a low frequency component at 60Hz, because the midpoint of DC-link capacitor is shared with the grid, and have a component at 120Hz due to single-phase power supply. For P4L converter, as the machine frequency at 20Hz, there is a harmonic component at 20Hz [shown Figs. 14(c) and 14(d)], since the phase 3 of the machine is also connected at the midpoint of the DC-link capacitor. Note that, the low frequency components are responsible of swinging of the DClink capacitor voltages, as shown in Figs. 12(d) and 13(d).

Moreover, RMS capacitor current of the P5L converter is always smaller than that of the P4L converter. When interleaved technique is applied, the high frequency components of the capacitor current are attenuated. The lowest value of the RMS capacitor current is obtained with the P5L converter with double-carrier PWM. A smaller value in the high frequency RMS capacitor current can increase the lifespan of the capacitor [18]. Similar analysis is achieved with the capacitor current  $i_{c2}$ . These outcomes are very close to the simulation results and theoretical analysis.

## X. CONCLUSIONS

In this paper two drive motor systems have been presented. These systems are composed of an AC-DC-AC single-phase to three-phase converter. The single-phase rectifier combines two parallel single-phase half-bridge converters without transformers. Suitable model and control strategy, including the PWM strategy have been developed.

Table V summarizes the comparison between conventional and proposed configurations for different figures of merit. In this table, the DC-link voltage, the WTHD and semiconductor power losses are normalized by conventional 5L topology.

The results for P5L and P4L configurations were obtained with double-carrier PWM, the condition that guarantees the lowest harmonic distortion. Among these configurations, the P5L topology presents the best performance, because it reduces: i) power losses, due to a reduction of the rectifier currents and ii) the harmonic distortion on the utility grid, when the interleaved technique is applied. Furthermore, this configuration uses only 15% more of DC-link voltage rating that the conventional 5L converter. The other drawback of the topology P5L is the use of a greater number of inductors compared with the conventional 5L one. On the other hand, the P4L topology (with double-carrier PWM implementation)



(a)

(b)



Fig. 13. Experimental results of the P4L2 converter. (a) Voltage and current of the grid. (b) Input currents of rectifiers A and B and circulating current. (c) DC-link voltage and load currents. (d) DC-link voltages.



Fig. 14. Experimental results - the spectrum of the capacitor current waveforms (a) P5L converter with single-carrier PWM. (b) P5L converter with double-carrier PWM. (c) P4L converter with single-carrier PWM. (d) P4L converter with double-carrier PWM.

reduces the harmonic distortion when compared with 3L converter and provides the same value of WTHD when compared with the conventional 5L converter.

switch currents of the rectifier and the irregular distribution of power losses among the switches of the rectifier and inverter circuits. Simulation and experimental results have been presented to illustrate the correct operation of the proposed

Additionally, the proposed systems permit to reduce the

	5L	3L	P5L	P4L
Number of Switch	10	6	10	8
DC-Link Rating	1	2	1.15	2
Rectifier Current Rating	1	1.06	0.5	0.52
Number of Inductor	1	1	2	2
WTHD	1	4.29	0.51	1
Power Losses	1	0.99	0.76	1.01

TABLE V COMPARISON OF ALL CONFIGURATIONS.

converters.

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### REFERENCES

- P. Enjeti, A. Rahman, and R. Jakkli, "Economic single-phase to threephase converter topologies for fixed and variable frequency output," *IEEE Trans. Power Electron.*, vol. 8, no. 3, pp. 329–335, Jul 1993.
- [2] F. Khosravi, N. Ahmad Azli, and A. Kaykhosravi, "Design of a reduced component count single-phase to three-phase quasi-z-source converter," *Power Electronics, IET*, vol. 7, no. 3, pp. 489–495, March 2014.
- [3] A. Gonzalez, C. Hernandez, and M. Arjona, "A novel high-efficiency parallel-winding connection for a three-phase induction motor fed by a single-phase power supply," *IEEE Trans. Energy Conversion*, vol. 29, no. 2, pp. 269–277, June 2014.
- [4] R. Machado, S. Buso, and J. Pomilio, "A line-interactive single-phase to three-phase converter system," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1628 –1636, nov. 2006.
- [5] E. Cipriano, C. Jacobina, E. da Silva, and N. Rocha, "Single-phase to three-phase power converters: State of the art," *IEEE Trans. Power Electron.*, vol. 27, no. 5, pp. 2437–2452, May 2012.
- [6] B. Lee, B. Fahimi, and M. Ehsani, "Overview of reduced parts converter topologies for AC motor drives," in *Proc. IEEE PESC*, vol. 4, 2001, pp. 2019–2024.
- [7] S. Bekiarov and A. Emadi, "A new on-line single-phase to three-phase ups topology with reduced number of switches," in *Proc. IEEE PESC*, vol. 1, June 2003, pp. 451–456.
- [8] P. Enjeti and A. Rahman, "A new single-phase to three-phase converter with active input current shaping for low cost AC motor drives," *IEEE Trans. Ind. Appl.*, vol. 29, no. 4, pp. 806 –813, jul/aug 1993.
- [9] C. B. Jacobina, E. C. dos Santos Jr., and M. B. R. Correa, "Control of the single-phase to three-phase four-leg converter for constant frequency output voltage," in *Proc. IEEE PESC*, 2005, pp. 52–58.
- [10] C. Jacobina, E. Cipriano dos Santos, M. de Rossiter Correa, and E. Cabral da Silva, "Single-phase-input reduced-switch-count AC-AC drive systems," *IEEE Trans. Ind. Appl.*, vol. 44, no. 3, pp. 789–798, May 2008.
- [11] R. S. Miranda, C. Jacobina, M. Correa, and A. Lima, "Reduced switch count dual-winding AC drive systems," in *Proc. IEEE PESC*, June 2005, pp. 726–732.
- [12] D.-C. Lee and Y.-S. Kim, "Control of single-phase-to-three-phase AC/DC/AC PWM converters for induction motor drives," *IEEE Trans. .Ind. Electron.*, vol. 54, no. 2, pp. 797 –804, april 2007.
- [13] J.-H. Choi, J.-M. Kwon, J.-H. Jung, and B.-H. Kwon, "High-performance online UPS using three-leg-type converter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 889–897, June 2005.
  [14] A. Bouscayrol, B. Francois, P. Delarue, and J. Niiranen, "Control
- [14] A. Bouscayrol, B. Francois, P. Delarue, and J. Niiranen, "Control implementation of a five-leg AC-AC converter to supply a three-phase induction machine," *IEEE Trans. Power Electron.*, vol. 8, no. 1, pp. 107–115, Jan. 2005.
- [15] R. Ramirez, J. Espinoza, P. Melin, M. Reyes, E. Espinosa, C. Silva, and E. Maurelia, "Predictive controller for a three-phase/single-phase voltage source converter cell," *IEEE Trans. Ind. Informatics*, vol. 10, no. 3, pp. 1878–1889, Aug 2014.
- [16] M. Baumann and J. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with dc-link current balancing," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3042– 3053, Dec. 2007.

- [17] T.-P. Chen, "Dual-modulator compensation technique for parallel inverters using space-vector modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 3004–3012, Aug. 2009.
- [18] L. Asiminoaei, E. Aeloiza, P. Enjeti, and F. Blaabjerg, "Shunt activepower-filter topology based on parallel interleaved inverters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175–1189, March 2008.
- [19] C. Jacobina, E. dos Santos, N. Rocha, and E. Fabricio, "Single-phase to three-phase drive system using two parallel single-phase rectifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1285 –1295, may 2010.
- [20] C. B. Jacobina, E. C. dos Santos, N. Rocha, and E. Fabricio, "Singlephase to three-phase five-leg converter based on two parallel singlephase rectifiers," in *Proc. IEEE IECON*, 3-5 Nov. 2009, pp. 850–855.
- [21] N. Rocha, C. Jacobina, E. dos Santos Jr., and R. Cavalcanti, "Parallel single-phase AC-DC-AC shared-leg converters: Modelling, control and analysis," *International Journal of Electrical Power & Energy Systems*, vol. 61, no. 0, pp. 27 – 38, 2014.
- [22] E. dos Santos, N. Rocha, and C. Brandao Jacobina, "Suitable singlephase to three-phase AC-DC-AC power conversion system," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 860–870, Feb 2015.
- [23] N. Rocha, E. de Menezes, I. de Oliveira, and C. Jacobina, "Single-phase to three-phase induction generation system with two parallel singlephase half-bridge converters," in *Proc. IEEE COBEP*, Oct. 2013, pp. 678–685.
- [24] R. M. Santos Filho, P. F. Seixas, P. C. Cortizo, L. A. B. Torres, and A. F. Souza, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2923–2932, Aug 2008.
- [25] C. B. Jacobina, M. B. de R. Correa, R. F. Pinheiro, E. R. C. da Silva, and A. M. N. Lima, "Modeling and control of unbalanced three-phase systems containing PWM converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 1807–1816, Nov./Dec. 2001.
- [26] Y.-K. Lo, T.-H. Song, and H.-J. Chiu, "Analysis and elimination of voltage imbalance between the split capacitors in half-bridge boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1175–1177, Oct 2002.
- [27] K. Rafal, M. Bobrowska, J. Barrena, and M. Kazmierkowski, "Component minimized AC/DC/AC converter with dc-link capacitors voltages balancing," in *EUROCON*, May 2009, pp. 861–866.
- [28] G. Covic, G. Peters, and J. Boys, "An improved single phase to three phase converter for low cost AC motor drives," in *Power Electronics* and Drive Systems, Feb 1995, pp. 549–554 vol.1.
- [29] G.-T. Kim and T. Lipo, "VSI-PWM rectifier/inverter system with a reduced switch count," *IEEE Trans. Ind. Appl.*, vol. 32, no. 6, pp. 1331– 1337, Nov 1996.
- [30] B. K. Bose, "Scalar decoupled control of induction motor," *IEEE Trans. Ind. Electron.*, vol. 20, pp. 216–225, Jan-Feb 1984.
- [31] D. Zhang, F. Wang, R. Burgos, R. Lai, and D. Boroyevich, "Interleaving impact on AC passive components of paralleled three-phase voltagesource converters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1042 – 1054, May/June 2010.
- [32] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 756–764, May/June 1996.
- [33] R. Wang, J. Zhao, and Y. Liu, "A comprehensive investigation of four-switch three-phase voltage source inverter based on double fourier integral analysis," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2774–2787, Oct 2011.
- [34] D. G. Holmesa and T. A. Lipo, Pulsewidth modulation for power converters: Principles and Practice. John Wiley & Sons, 2013.
- [35] F. Casanellas, "Losses in PWM inverters using IGBTs," *Electric Power Applications, IEE Proceedings* -, vol. 141, no. 5, pp. 235–239, Sep 1994.
- [36] L. Mestha and P. Evans, "Analysis of on-state losses in PWM inverters," *Electric Power Applications, IEE Proceedings B*, vol. 136, no. 4, pp. 189–195, Jul 1989.
- [37] Z. Ivanovic, B. Blanusa, and M. Knezic, "Analytical power losses model of boost rectifier," *IET Power Electron.*, vol. 7, no. 8, pp. 2093–2102, August 2014.
- [38] J. Dias, E. dos Santos, C. Jacobina, and E. da Silva, "Application of single-phase to three-phase converter motor drive systems with IGBT dual module losses reduction," in *COBEP*, vol. 1, Bonito, MS, Brazil, 27-01 set./Oct. 2009, pp. 1155 – 1162.
- [39] M. Cavalcanti, E. da Silva, D. Boroyevich, W. Dong, and C. Jacobina, "A feasible loss model for igbt in soft-switching inverters," in *PESC*, vol. 3, 15-19 June 2003, pp. 1845 – 1850.